

MAINTENANCE INTERFACE UNIT FOR SERVICING
MULTIPROCESSOR SYSTEMS

ABSTRACT

An apparatus containing a maintenance interface unit is described. In one exemplary implementation, the apparatus includes a multiprocessor system and the maintenance interface unit. The multiprocessor system uses cache coherency for accessing memory. The maintenance interface unit is integrated within the multiprocessor system and is configured to provide a backdoor accessibility to the multiprocessor system on-behalf of a peripheral maintenance system. The maintenance interface unit is also configured to perform operations within the multiprocessor system while maintaining the cache coherency.